

Application No. 10/646988 (Docket: CNTR.2209)
37 CFR 1.111 Amendment dated 01/30/2008
Reply to Office Action of 10/30/2007

AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0009] In accordance with one embodiment of the present invention, an apparatus within a microprocessor is provided including a plurality of functional units each having an activity output for indicating when a respective functional unit is enabled, and for dynamically indicating how much power the respective functional unit is consuming. The apparatus also includes utilization assessment logic, coupled to the activity outputs of the functional units, for assessing activity thereof to determine a current total power consumption value for the processor. The apparatus further includes power control logic, coupled to the utilization assessment logic, for comparing the current total power consumption value with a threshold power value included in a selected power profile, where a select signal directs the power control logic to select the specified power profile from a plurality of power profiles stored within the power control logic. The apparatus still further includes a power consumption controller, coupled to the power management logic and the functional units, for engaging one of a plurality of power reduction modes if the current total power consumption value exceeds a threshold power value of the selected power profile.

[0010] In accordance with another embodiment of the present invention, a processor is provided which includes a plurality of functional units each having an activity output for indicating when the respective functional unit is active. The processor further includes utilization assessment logic, coupled to the activity outputs of the functional units, for assessing activity thereof to determine a current total power consumption value for the processor. The processor also includes power control logic, coupled to the utilization assessment logic, for comparing the current total power consumption value with a threshold power value included in a selected power profile, where the selected power profile is selected from a plurality of power profiles stored within the power control logic. The processor still further includes a power consumption controller, coupled to the

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power control logic, for disabling a first functional unit of the plurality of functional units to reduce the processor's power consumption if the current total power consumption value exceeds the threshold power value of the selected power profile.

[0011] In accordance with yet another embodiment of the present invention, a microprocessor power management mechanism within a microprocessor is provided which includes a plurality of functional units each having an activity output for indicating when a respective functional unit is enabled, and for dynamically indicating how much power the respective functional unit is consuming. The microprocessor power management mechanism further includes power management logic, coupled to the activity outputs of the functional units, for assessing the activity of individual functional units to determine a current total power consumption value for the microprocessor. The microprocessor power management mechanism also includes a power consumption controller, coupled to the power management logic and the functional units, for disabling at least one of the functional units, if the current total power consumption value exceeds a threshold power value of a selected power profile, where the selected power profile is selected from a plurality of power profiles stored within the power consumption controller, and where a select signal directs the power consumption controller to select the one of a plurality of power profiles.

[0012] A method is also disclosed for operating the described processor which includes a plurality of functional units. The disclosed method includes selecting a power profile for the processor from a plurality of power profiles each having a respective threshold power value associated therewith, thus providing a selected power profile. The method additionally includes storing the plurality of power profiles within the microprocessor. The method additionally includes dynamically indicating how much power each of the individual functional units is consuming. The method also includes assessing activity by individual functional units of the processor to determine a current total power consumption value for the processor. The method further includes comparing the current total power consumption value with the threshold power value of the selected power profile. The method still further includes engaging one of a plurality of power reduction

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modes if the current total power consumption value exceeds the threshold power value of the selected power profile.

[0013] Another embodiment of the method includes selecting a power profile for the processor from a plurality of power profiles each having a respective threshold power value associated therewith, thus providing a selected power profile. The method also includes assessing activity by individual functional units of the processor to determine a current total power consumption value for the processor. The method further includes comparing the current total power consumption value with the threshold power value of the selected power profile. The method still further includes disabling a first functional unit of the plurality of functional units to reduce the processor's power consumption if the current total power consumption value exceeds the threshold power value of the selected power profile.

[0014] The disclosed processor advantageously achieves reduced power consumption. The amount of power conservation exhibited by the processor is selectable according to user specified power profiles. Other features and advantages of the present invention will become apparent upon study of the remaining portions of the specification and drawings.